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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,648	07/27/2004	David L. DeMaris	BUR920040058US1	4647

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
12/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOCommunications@hwdpatents.com

Office Action Summary	Application No.	Applicant(s)	
	10/710,648	DEMARIS ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-11,14-17 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/27/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 5-6 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim 5 recites the limitation "the combining step" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites “n choose matrices” in lines 2-3 which is unclear. Does applicant mean to claim “n chosen k matrices”? Clarify

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 9-11, 14-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeuchi (US Patent 6,952,818) in view of Radecka, K., et al., "Design verification by test vectors and arithmetic transform universal test set".

4. As for the claims Ikeuchi discloses the invention substantially as claimed, including

1. A method of synthesizing layout patterns, comprising the steps of:
Forming a set of test patterns, and mapping the test patterns to a test pattern set [col. 5, lines 33-60; col. 6, lines 27-37; col. 10, line 54 – col. 11, line 20; col. 12, line 66 – col. 13];

Ikeuchi does not specifically disclose
embodying Walsh patterns in a set of Walsh pattern matrices;
processing at least one from the set of Walsh pattern matrices to form a set of test matrices; and
mapping the set of test matrices to a test pattern set [];

Radecka discloses the use of Walsh pattern matrices for use of verification and mapping those test matrices to test patterns (through superposition) [section 5. "Bounding error through Walsh-Hadamard Transform"; section 6. "Experimental results"].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ikeuchi and Radecki because utilizing a Walsh-Hadamard transform for forming pattern matrices, forming test matrices, and mapping to a test pattern set within Ikeuchi's system would have provided Ikeuchi's system with a method of a known algorithm for improving pattern and error recognition for the purpose of improving layout synthesis.

10. A system for generating a set of test patterns to test an optical proximity correction algorithm [Ikeuchi, col. 5, lines 33-60; col. 6, lines 27-37; col. 10, line 54 – col. 11, line 20; col. 12, line 66 – col. 13],

Ikeuchi does not specifically disclose the system comprising:
a system that generates a set of Walsh pattern matrices; a system that processes groups of matrices from the set of Walsh pattern matrices to form a set of test matrices []; and
a system that maps the set of test matrices to a test pattern set [];

Radecka discloses the use of Walsh pattern matrices for use of verification and mapping those test matrices to test patterns (through superposition) [section 5. "Bounding error through Walsh-Hadamard Transform"; section 6. "Experimental results"].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ikeuchi and Radecki because utilizing a Walsh-Hadamard transform for forming pattern matrices, forming test matrices, and mapping to a test pattern set within Ikeuchi's system would have provided Ikeuchi's system with a method of a known algorithm for improving pattern and error recognition for the purpose of improving layout synthesis.

15. A program product stored on a recordable medium for generating a set of test patterns to test an optical proximity correction algorithm [col. 5, lines 33-60; col. 6, lines 27-37; col. 10, line 54 – col. 11, line 20; col. 12, line 66 – col. 13],

Ikeuchi does not specifically disclose the program product comprising:
means for generating a set of Walsh pattern matrices; means for processing groups of matrices from the set of Walsh pattern matrices to form a set of test matrices;

means for mapping the set of test matrices to a test pattern set [];

Radecka discloses the use of Walsh pattern matrices for use of verification and mapping those test matrices to test patterns (through superposition) [section 5. "Bounding error through Walsh-Hadamard Transform"; section 6. "Experimental results"].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ikeuchi and Radecka because utilizing a Walsh-Hadamard transform for forming pattern matrices, forming test matrices, and mapping to a test pattern set within Ikeuchi's system would have provided Ikeuchi's system with a method of a known algorithm for improving pattern and error recognition for the purpose of improving layout synthesis.

2. The method of claim 1, wherein the set of Walsh pattern matrices are generated using an Nth order Hadamard matrix, wherein N dictates the size of each matrix [Radecka, sections 5 and 6];

3. The method of claim 1, wherein the processing step utilizes a Boolean operation [Radecka, sections 5 and 6];

4. The method of claim 3, wherein the Boolean operation utilizes at least one logical operation selected from the group consisting of: a logical or, logical nor, logical and, and logical nand [Radecka, sections 5 and 6];

5. The method of claim 1, wherein the combining step determines a set of combinatorial indices for n choose k matrices, wherein n represents the number of matrices in the set of Walsh pattern matrices, and k is the number of matrices in a group of processed matrices [Radecka, section 5, for n and k];

9. The method of claim 1, comprising the further step of pruning the pattern set based on a predetermined set of rules [Radecka, section 4.2, obtaining a reduced matrix according to error check matrix];
11. The system of claim 10, wherein the processing system determines a set of combinatorial indices for n choose k matrices, wherein n represents the number of matrices in the set of Walsh pattern matrices, and k is the number of matrices in each group of matrices [Radecka, section 5, for n and k];
14. The method of claim 10, further comprising a system for pruning the pattern set based on a predetermined set of rules [Radecka, section 4.2, obtaining a reduced matrix according to error check matrix];
16. The program product of claim 15, wherein the combining means determines a set of combinatorial indices for n choose k matrices, wherein n represents the number of matrices in the set of Walsh pattern matrices, and k is the number of matrices in each group of matrices [Radecka, sections 5 and 6];
17. The program product of claim 15, wherein the processing means processes matrices using a Boolean operation [Radecka, sections 5 and 6];
20. The program product of claim 15, further comprising means for pruning the pattern set based on a predetermined set of rules [Radecka, section 4.2, obtaining a reduced matrix according to error check matrix].

5. Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. Claims 7-8, 12-13, and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination the invention as claimed, including the method, system, and computer program product comprising at least the steps, system or means for 6. The method of claim 5, wherein k is selected as large as possible given a set of computational constraints;
7. The method of claim 1, wherein the mapping step maps matrix entries to tiles in a minimum space, minimum width grid, wherein each tile is assigned a value of either level on or level off; 8. The method of claim 7, wherein the mapping step adjusts spacing of tiles when a transition from on to off, or off to on is detected; 12. The system of claim 10, wherein the mapping system maps matrix entries to tiles in a minimum space, minimum width grid, wherein each tile is assigned a value of either level on or level off; 13. The method of claim 12, wherein the mapping system adjusts spacing of tiles when a transition from on to off, or off to on, is detected; 18. The program product of claim 15, wherein the mapping means maps matrix entries to tiles in a minimum space, minimum width grid, wherein each tile is assigned a value of either level on or level off; and 19. The program product of claim 18, wherein the mapping means adjusts spacing of tiles when a transition from on to off, or off to on, is detected.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/
Primary Examiner
Art Unit 2825

SAW
December 3, 2007